In the Claims

1-29. (Cancelled)

30. (Original) A method of bonding two structures together, the method comprising:

depositing low temperature grown semiconductor bonding layers on first and second structures to form a combined structure;

placing the bonding layers in contact with each other;

applying pressure to the combined structure; and

annealing the combined structure under conditions sufficient for the bonding layers to bond the first and second structures together.

31. (Original) The method of claim 30, further comprising applying the pressure substantially uniformly to the combined structure during annealing.

32. (Original) The method of claim 30, wherein the annealing of the combined structure occurs under conditions sufficient for the bonding layers to form a polycrystalline material.

33. (Original) The method of claim 30, wherein the bonding layer comprises at least one of amorphous and polycrystalline (Ga,As) and the annealing of the combined structure occurs at a temperature of between about 300°C and 500°C and for a time sufficient for the bonding layers to form a (Ga,As) material that is substantially entirely polycrystalline.

34. (Original) The method of claim 30, wherein the bonding layer comprises at least one of amorphous and polycrystalline (Ga,P) and the annealing of the combined structure occurs at a temperature of between about 500°C and 700°C and for a time sufficient for the bonding layers to form a (Ga,P) material that is substantially entirely polycrystalline.

35. (Original) The method of claim 30, wherein the bonding layer comprises at least one of amorphous and polycrystalline (Ga,N) and the annealing of the combined

structure occurs at a temperature of between about 700°C and 900°C and for a time sufficient for the bonding layers to form a (Ga,N) material that is substantially entirely polycrystalline.

36. (Original) The method of claim 30, wherein the bonding layers are placed in contact with each other without regard for a relative angular orientation of the first and second structures to each other.

37. (Original) The method of claim 30, wherein at least one of the first and second structures comprises a non-semiconductor substrate.

38. (Original) The method of claim 30, further comprising fabricating at least one of an electronic and optoelectronic device from the combined structure.

39. (Original) The method of claim 30, wherein the annealing of the combined structure occurs under conditions that are not damaging to the first and second structures but are sufficient to form bonds that are strong enough to survive subsequent processing at temperatures higher than that used during the bonding.

40. (Original) The method of claim 30, wherein a bonding interface produced by the annealing is substantially optically transparent to light emitted by the combined structure.

41. (Original) The method of claim 30, wherein a bonding interface produced by the annealing is strong enough to be substantially unaffected by processing of the combined structure.

42. (Original) The method of claim 30, wherein the deposition deposits between about 3 nm and about 600 nm of material on each of the first and second structures.

43. (Original) The method of claim 30, wherein the deposition deposits at least one of low temperature grown (Ga,As), (Ga,P) and (Ga,N) on at least one of the first and second structures.

44. (Original) The method of claim 30, further comprising selecting a composition of the bonding layer such that an amorphous layer is deposited on at least one of the first and second structures.

45. (Original) The method of claim 44, wherein the annealing of the combined structure occurs under conditions sufficient for the bonding layers to form a polycrystalline material from the amorphous layer.

46. (Original) The method of claim 30, further comprising selecting a composition of the bonding layer such that a polycrystalline semiconductor layer is deposited on at least one of the first and second structures.

47. (Original) The method of claim 46, wherein the annealing of the combined structure occurs under conditions sufficient for the bonding layers to recrystallize into a polycrystalline material.

48. (Original) The method of claim 30, wherein the annealing occurs at temperatures of at most about 800°C.

49. (Original) The method of claim 30, wherein the bonding layer comprises a compound semiconductor.

50. (Original) The method of claim 49, further comprising doping the bonding layer with Si.

51. (Original) The method of claim 49, further comprising doping the bonding layer with a dopant that helps to control morphology of the compound semiconductor.

52. (Currently Amended) The method of claim 30, wherein ~~Ga-rich low temperature-grown semiconductor bonding layers are deposited~~the first and second structures are separate structures from each other before the bonding layers are placed in contact and the combined structure is annealed.

53. (Original) The method of claim 30, the bonding layer is deposited by molecular beam epitaxy (MBE) at a temperature of at most about 100°C.

54-71. (Cancelled)

72. (Withdrawn) The method of claim 30, wherein the bonding method is used in fabrication of a photodiode.

73. (Withdrawn) The method of claim 30, wherein the bonding method is used in fabrication of a transistor.

74. (Withdrawn) The method of claim 73, wherein the transistor is a heterojunction bipolar transistor.

75. (Withdrawn) The method of claim 73, wherein the transistor is a high-electron-mobility transistor.

76. (Withdrawn) The method of claim 30, wherein the bonding method is used in fabrication of a light-emitting diode.

77. (Withdrawn) The method of claim 30, wherein the bonding method is used in fabrication of a laser.

78. (Previously Presented) The method of claim 30, wherein at least one of the first and second structures comprises a semi-insulating substrate.

79. (Previously Presented) The method of claim 30, wherein at least one of the first and second structures comprises an insulator.

80. (Previously Presented) The method of claim 30, wherein at least one of the first and second structures comprises a pseudomorphic structure.

81. (Withdrawn) The method of claim 30, wherein at least one of the first and second structures comprises a multiple quantum well structure.

82. (Previously Presented) The method of claim 30, wherein the bonding layer is devoid of polymers, ceramics, and metals.

83-100. (Cancelled)

101. (Previously Presented) A method of bonding two structures together, the method comprising:

depositing Ga-rich low temperature grown compound semiconductor bonding layers on first and second structures to form a combined structure;

placing the bonding layers in contact with each other;

applying pressure to the combined structure; and

bonding the first and second structures together by annealing the combined structure.

102. (New) A method of bonding two structures together, the method comprising:

depositing low temperature compound semiconductor bonding layers on separate first and second structures;

placing the bonding layers of the separate first and second structures in contact with each other;

applying pressure to a combined structure of the first and second structures and the bonding layers; and

annealing the combined structure under conditions sufficient for the bonding layers to bond the first and second structures together.

103. (New) The method of claim 102, further comprising applying the pressure substantially uniformly to the combined structure during annealing.

104. (New) The method of claim 102, wherein the annealing of the combined structure occurs under conditions sufficient for the bonding layers to form a polycrystalline material.

105. (New) The method of claim 102, wherein the bonding layer comprises at least one of amorphous (Ga,As) and polycrystalline (Ga,As) and the annealing of the combined structure occurs at a temperature of between about 300°C and 500°C and for a time sufficient for the bonding layers to form a (Ga,As) material that is substantially entirely polycrystalline.

106. (New) The method of claim 102, wherein the bonding layer comprises at least one of amorphous (Ga,P) and polycrystalline (Ga,P) and the annealing of the combined structure occurs at a temperature of between about 500°C and 700°C and for a time sufficient for the bonding layers to form a (Ga,P) material that is substantially entirely polycrystalline.

107. (New) The method of claim 102, wherein the bonding layer comprises at least one of amorphous (Ga,N) and polycrystalline (Ga,N) and the annealing of the combined structure occurs at a temperature of between about 700°C and 900°C and for a time sufficient for the bonding layers to form a (Ga,N) material that is substantially entirely polycrystalline.

108. (New) The method of claim 102, wherein at least one of the first and second structures comprises a non-semiconductor substrate.

109. (New) The method of claim 102, wherein the annealing of the combined structure occurs under conditions that are not damaging to the first and second structures but are sufficient to form bonds that are strong enough to survive subsequent processing at temperatures higher than that used during the bonding.

110. (New) The method of claim 102, wherein a bonding interface produced by the annealing is substantially optically transparent to light emitted by the combined structure.

111. (New) The method of claim 102, wherein at least one of low temperature grown (Ga,As), (Ga,P) and (Ga,N) is grown on at least one of the first and second structures.

112. (New) The method of claim 102, further comprising selecting a composition of the bonding layer such that an amorphous layer is deposited on at least one of the first and second structures.

113. (New) The method of claim 112, wherein the annealing of the combined structure occurs under conditions sufficient for the bonding layers to form a polycrystalline material from the amorphous layer.

114. (New) The method of claim 102, further comprising selecting a composition of the bonding layer such that a polycrystalline semiconductor layer is deposited on at least one of the first and second structures.

115. (New) The method of claim 114, wherein the annealing of the combined structure occurs under conditions sufficient for the bonding layers to recrystallize into a polycrystalline material.

116. (New) The method of claim 102, wherein the annealing occurs at temperatures of at most about 800°C.

117. (New) The method of claim 102, further comprising doping the bonding layer.

118. (New) The method of claim 102, wherein the bonding layers are placed in contact with each other without regard for a relative angular orientation of the first and second structures to each other.

119. (New) The method of claim 102, the bonding layer is deposited by molecular beam epitaxy (MBE) at a temperature of at most about 100°C.